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High Density of Deep Acceptor Traps near the 4H-SiC Conduction Band Limits Surface Mobility and Dielectric Breakdown Field in an n-channel 4H-SiC MOSFET

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Abstract: *The oxide fixed charge density N_f and density of near interface traps D_{NIT} has been calculated from reliable samples of 4H-SiC MOS devices in a collaborative effort. The N_f in the p-type MOS device equals the D_{NIT} on the n-type MOS device after NO annealing of the wet oxide, indicating that they are a result of ionisation of deep traps formed due to neutral oxygen vacancies near the Si-rich 2-3 nm SiC/SiO_2 interface region. The value of N_f is 23.6 x 10^{11}/cm^2. This is high and significantly contributes to limiting mobility of the n-channel MOSFET. The oxide breakdown strength is also affected by high N_f values and therefore needs to be monitored along with the mobility. A H_2 annealing after NO annealing has shown a further increase in FE surface mobility to55 cm^2/V-s and is the result of reduced D_{NIT} after H_2 annealing. However, a lower oxide breakdown is reported after H_2 anneal at about 5MV/cm. The oxide breakdown field of 7.8 MV/cm with charges is obtained after NO annealing. Another competitive device is a result of N_2 annealing at high temperatures giving a peak surface field effect mobility of 50cm^2/V-s before N_2 anneal and a peak mobility range of 25-35 cm^2/V-s after N_2 anneal with an oxide breakdown field greater than 8MV/cm. The annealing gas is environment-friendly and forms strong Si-N bonds. It is possible to reduce D_{NIT} further by high temperature oxidation, but it also increases D_{it} at E_c-0.2 eV at the same time, which can be passivated with N. It is also possible to reduce D_{it} further by increasing the N concentration at the interface during NO annealing.*

Keywords: *Deep Traps, Silicon Carbide FET, Conduction band, Mobility, Dielectric Breakdown field*

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I. Introduction

This report is another sequel to the two previous reports by the author as part of the collaborative group study [1-4]. In this report, a new calculation is made on the p-type 4H-SiC-Si-face (0001) MOS device from the data set of the author's collaborative study [1-2, 5-6] and is presented in a Table below. Before opening discussion on the data in the Table, the three types of interface traps existing in the SiC/SiO_2 system are distinguished. One is at the interface only, and arises from the so-called P_b centres or P_{bC} centres [7]. A P_b centre is Si atom connected to three Si atoms at the interface with one dangling bond or a dangling bond on the second Si atom connected to the Si atom below it. These are known as P_{b0} and P_{b1} in the Si technology where their density is about 10^{12}/cm^2 on the p (100) surface [8]. The density of P_{b1} is less than the density of P_{b0}. The P_{bC} centres are carbon-dangling bonds on the 4H-SiC surface. There density is found to be 3-4 x 10^{12}/cm^2 [9]. The Si/SiO_2 system has only P_b centres but the SiC/SiO_2 system has both P_b and P_{bC} centres due to Si and C dangling bonds. They can acquire a positive, negative or zero charge and are therefore amphoteric. There is another type of interface traps in the SiC/SiO_2system that arise due to sp^2-bonded carbon clusters and graphite like carbon [10]. These are mainly donor states or hole traps in the lower half of the SiC bandgap with the intrinsic Fermi level shown to be at E_c-0.97 eV in 4H-SiC due to intrinsic defect density of 1.1 x 10^{14}/cm^3 [11, 12]. Being donor states, they are neutral when occupied with electrons and become positive upon donating an electron or capturing a hole. These add positive charges to p-type MOS device when the Fermi level is near the VB and when the donor states are empty and therefore positively charged. If donor states due to sp^2 bonded carbon and graphite like carbon are reduced in number because they are oxidised, then the P_b centres will take their place as donor states. High temperature inert anneal in N_2 or Ar gas has high density of donor states and low temperature inert anneal has low density of donor states, so N_f is accordingly higher or lower due to inert anneals [8, 13-14]. The small upper half of the 4H-SiC bandgap of 0.97 eV above the intrinsic Fermi level also has acceptor states coming from sp^2 bonded carbon and graphite like carbon that have been shown to be passivated by NO annealing and add to the traps near VB [3]. The acceptor states are negative when occupied and neutral when empty. The donor states occupy almost two-thirds of the 4H-SiC bandgap below the intrinsic Fermi level are much larger in density with the sp^2 bonded carbon states starting from E_v + 1.4 eV [10]. The above two types of interface traps are represented as D_{it}. The contribution to D_{it} from the P_b centres is not

observed in 4H-SiC/SiO_2system by Afanasev et al. [10]. However, after wet re-oxidation [15], the donor states are reduced and acceptor states are increased as observed in Fig. 2 of the report by Williams et al. [3] making the D_{it} distribution asymmetric after re-oxidation. The third type of traps at the SiC/SiO_2 interface are called "border" traps, which are present in the oxide within about 3 nm of the interface and can exchange charge with the Si or SiC CB [16-17]. These are represented as D_{bt} or D_{NIT}. It is difficult to distinguish between the three types of traps by electrical characterisation methods except the fact that border traps are dominant at low frequencies of less than 100 Hz [18-19]. It is to be noted that D_{it} at E_c-0.2 eV is not necessarily the same as D_{NIT} near CB of the semiconductor unless D_{it} is passivated substantially. In the as oxidised dry or wet oxide on Si-face of 4H-SiC having (0001) orientation, the D_{it} at E_c-0.2 eV is at 2.4 x $10^{12}/cm^2eV$ with Ar annealing gas containing small parts of oxygen [3, 20]. Wet re-oxidation at 950^{o}C for 3 hrs has shown to reduce the donor states and increase the acceptor states as mentioned earlier [3]. Wet re-oxidation has also shown to reduce near-midgap interface states density and the fixed charge density in p-6H-SiC-Si-face MOS devices having (0001) orientation [21-22].

Silicon has a diamond lattice structure that belongs to cubic crystal family. It can be seen as two interpenetrating face-centred-cubic (fcc) sub-lattices with one sub-lattice displaced from the other by one quarter of a distance along a diagonal of a cube, that is, a displacement of a $\sqrt{3}/4$ [23]. The planar density (PD) of atoms on the Si (100) and Si (110) and Si (111) surface can be calculated by knowing the number of atoms on the plane and dividing by the area of the plane. The lattice constant for Si is 0.543 nm denoted by 'a'. The number of atoms on the three faces are 2 on each face, and the areas of the planes are a^2, $a\sqrt{}$ 2a, and $\{(1/2) \times (\sqrt{2}a) \times ((\sqrt{2}a\ (\sqrt{3}/2)) = a^2\sqrt{3}/2\}$, giving PDs tabulated below in Table I. The area of a hexagonal plane is given by 2 times the area of a trapezoid having two parallel sides as 'a' and '2a' and a height of ($a\sqrt{3}/2$). This equals ($3\sqrt{3}/2$) a^2. PD for the hexagonal closely packed (hcp) crystal plane of 6H-SiC or 4H-SiC having (0001) surface orientation is therefore given as below in Table I. It can be observed that the density of atoms on 4H-SiC (0001) face is nearly the same as on Si (111) face. The comparison of N_f values in oxides on 4H-SiC MOS devices should therefore be made with those in oxides grown on Si (111) face. This has been mentioned by the research group of Afanasev et al. also [10]. On a clean semiconductor surface, the PD represents P_b centres which act as surface recombination centres. These states on Si surface reduce to 10^{11}-$10^{12}/cm^2$ after oxidation [24-26].

Table I. Planar density of atoms on the Si cubic faces and on 6H- and 4H-SiC (0001) hcp faces.

Si(100) (x $10^{14}/cm^2$)	Si(110) (x $10^{14}/cm^2$)	Si(111) (x $10^{14}/cm^2$)	6H-or 4H-SiC (0001) hcp plane (x $10^{14}/cm^2$)	Ratio of PD Si(111)/Si(100)	Ratio of PD Si(100)/Si(110)	Ratio of PD of 4H-SiC (0001)/Si(111)	Ratio of PD of 4H-SiC (0001)/Si(100)
6.7	4.8	7.8	8.1	1.16	1.4	1.04	1.21

II. Results and Discussion

A new calculation is made on the p-type 4H-SiC-Si-face (0001) MOS device from the data set of the author's collaborative study [1-6] and is presented in the Table II below. The flat band voltage for the p-type MOS device is determined from the high frequency (HF) 1 MHz C-V trace. It is observed to be – 6V [2]. The device had Au contact at the gate having a work function of 5.1 eV. The p-4H-SiC doped with 9.1 x $10^{16}/cm^3$ Al as p-type impurity [15] has a work function of 6.8 eV. Therefore the metal-semiconductor work function difference comes out to be -1.7 eV, which in terms of voltage is -1.7 V. The flat band voltage for only the charges in the oxide is therefore (-6V – (-1.7V)) = -4.3 V. For an oxide capacitance of 80 pF for 40 nm oxide) [5], N_f can be given as:

$$N_f = C_{ox}V/(qA)$$
$$N_f = (80 \times 10^{-12}\ F) \times (-4.3\ V) / ((1.602 \times 10^{-19} coul) \times (9.1 \times 10^{-4}\ cm^2)) = 23.6 \times 10^{11}/cm^2.$$

Table II. The observed and calculated parameters from n- and p- 4H-SiC MOS devices in accumulation and inversion from the author's collaborative study. The oxides are annealed in NO at 1150^{o}C for 2 hrs [1-6].

4H-SiC-Si-face (0001) oriented MOS device in accumulation	NO annealed oxide thickness (nm)	Leakage current density, (A/cm^2), $J_{D,ox}$ = 8.6 x 10^{-9}	Flat band Voltage, (V)	Fixed charge density, N_f (cm^{-2}) (x 10^{11})	Near Interface Trap density,D_{NIT} ($cm^{-2}eV^{-1}$) (x 10^{11})	Surface effective mobility for n-channel MOSFET, (cm^2/V-s)	Oxide Breakdown without charges, (MV/cm)	Oxide Breakdown with charges, (MV/cm)
n-type	40	8.8 x 10^{-10}	< 1	-24before NO Negligible after NO	23.5 After NO		7.8	7.8
p-type	40	8.8 x 10^{-9}	- 6	12 before NO 23.6 after NO	NIL (D_{it} exists)	30-35	9.5	7.8

The NITs and positive fixed charges are mostly coming from the neutral oxygen vacancies in the oxide, where it is believed that a hole capture by the neutral oxygen vacancy can ionise the trap and create E' centre and a positive hole charge centre [27]. This is discussed next. The grown and NO annealed oxide in the devices of Table II are 40 nm thick [1, 5]. Table II also presents the displacement current density ($J_{D,ox}$) for 40 nm thick SiO_2 as 8.6 x 10^{-9} A/cm^2, keeping in mind that $J_{D,ox}$ depends on the oxide thickness and needs to be calculated separately for each sample [5, 6]. The observed leakage current density in the n-type MOS device in accumulation is 8.8x 10^{-10} A/cm^2. This is one order less than the $J_{D,ox}$, indicating the presence of NITs in the oxide near CB [5]. At the same time, there is a negligible N_f after NO annealing as the flat band voltage is at less than 1 V, and with the Mo-n-4H-SiC work function difference of 4.7-3.9 equalling 0.8 V, leaves no voltage for the charges. In the p-type MOS device, the observed leakage current is same as the $J_{D,ox}$ at 8.8 x 10^{-9} A/cm^2 indicating that there are no NITs near the VB. Instead, a positive fixed charge density N_f is calculated from the flat band voltage of -6 V to be 23.6 x 10^{11}/cm^2. The n-type device has NITs near CB and the p-type device has no NITs near the VB. Both have some fixed charges with the n-type device having negligibly small density. Also, D_{NIT} in the n-type device is same as the N_f in the p-type device at 300 K. This is the situation after NO annealing of the oxide at 1150^{o}C for 2 hrs.

The neutral oxygen vacancy is a common defect occurring in the SiO_2 with one of the bridging oxygen missing from the SiO_4 tetrahedron and then the two neighbouring tetrahedrons bonded with the Si-Si bond as shown earlier. This can constitute the SiO_x. The diamagnetic neutral oxygen vacancies in SiO_2, forming SiO_x with $0 < x < 2$ and symbolised as $\equiv Si - Si \equiv$, ionises upon irradiation with high energy radiation such as X-rays, γ-rays, neutrons and Ultra Violet rays or by capturing a hole, into paramagnetic defects as E' centre (unpaired electron) and a positive charge (hole) centre in the oxide. These have been detected in 1956 by Weeks [27] using the Electron Paramagnetic Resonance (EPR) technique. The E' centre is originally located at 5.85 eV and is now accepted to be at 5.83 eV from the VB of SiO_2, with some confusion existing around 5.7-5.9 eV [28] and the neutral oxygen vacancy is located at 7.6 eV from the VB of SiO_2. Weeks pointed to the first paper by Faraday in 1825 on colouration of glass by solar radiation. The above defects have been studied in great details in the last fifty years and the author limits himself to the basics only, as learnt from the scientific literature and review articles [28-30]. As can be observed from the data of Table II above, D_{NIT} and N_f values are equal and is believed to be the result of hole capture by the neutral oxygen vacancy forming the E' centre and the positive charge, with the E' centre representing D_{NIT} and the positive charge representing N_f with their densities equal because they are created from the same neutral oxygen vacancy. Neutral oxygen vacancy is a common defect in SiO_2. It is diamagnetic and cannot be detected by EPR technique. The E' centre acts as a capacitor in series with oxide capacitance with the n-MOS device in accumulation and reduces the total equivalent series capacitance, thereby lowering the low-field leakage current. The same neutral oxygen vacancy becomes a positive charge centre by capturing a hole say, when the n-MOS device is in depletion or a p-MOS device is in accumulation and an E' centre located at 5.85 eV from the SiO_2 VB or 3.05 eV from the SiO_2 CB as a deep electron trap or acceptor trap being negative with one unpaired electron. A study has shown the E' centre dominates the hole trapping in a good quality silicon dioxide [31]. The positive charge created cannot become a trap capacitance with accumulated holes in the VB as they are 'like' charges and a linear capacitance has opposite charges across its plates, and is part of the oxide. So, no NITs exist near the VB. This will be true for both 4H-SiC and Si-MOS device. The SiO_2/4H-SiC interface is complicated with C and N involved. All C is bonded to N after NO annealing and the energy level goes to the VB of 4H-SiC [3]. Furthermore, after NO annealing, N replaces O at the interface making the interface SiN_x or SiON or Si-C-O-N type [5, 32-33].

Continuing further, the field at the anode is reduced for hole tunnelling in the p-type MOS device in accumulation due to the presence of positive charges giving lower hole current. The slope constant for FN hole tunnelling however is the same as that of n-MOS device in accumulation and therefore the oxide breakdown field with charges is the same at 7.8 MV/cm. If the oxide field is corrected for the positive charges, the oxide breakdown field for hole tunnelling increases to 9.5 MV/cm without charges [2, 5]. These breakdown fields are presented in the Table II above. Thus, there are NITs in the CB but negligible fixed charges in the n-MOS device. There are no NITs in the VB of the p-type MOS device but there are positive fixed charges equal in density to the density of NITs in the n-type device near the CB. That is, where there are switching states near CB of Si and 4H-SiC, there are negligible fixed states, and where there are no switching states near the VB of Si and 4H-SiC, there are some fixed states. This is the case after NO annealing and including nitrogen into the 4H-SiC/SiO_2system. In 1992, border traps or NITs have been introduced as part of the oxide charges within about 3 nm in the oxide from the interface that can exchange charge with the Si CB [16]. These traps can be treated as part of the oxide with the MOS in accumulation [5, 6] or part of the interface traps with the MOS device in depletion. Treating them as part of the oxide is a new idea introduced by the author. When treated as part of the oxide, the trap capacitance is in series with the oxide capacitance lowering the equivalent series capacitance and lowering the low-field leakage current [5, 6]. When treated as part of the interface traps with the MOS device in depletion, the trap capacitance gets added to the interface trap capacitance in parallel and increases the quasi-

static capacitance at low frequency creating a 'hump' in the low frequency C-V curve [5, 6, 18, 19, 34]. The 'hump' can be seen in Fig. 2 of Williams et al. [3], presenting D_{it} distribution after wet re-oxidation [3]. The D_{NIT} obtained is in experimental agreement with the D_{NIT} obtained when treated as part of the interface traps with the p-MOS device in strong inversion as an n-channel MOSFET [1, 34]. However, there are some fixed charges, also within the 2 nm of the oxide /semiconductor interface which are different from the deep traps acting as fixed charges with the p-MOS device in accumulation. There density is very low particularly in the 4H-SiC MOS devices because the deep trap densities are high in the low 1012 order. These have been discussed earlier.

The N_f for different combinations of atoms on the E' centre are summarised in Table III below. An EELS study confirms the formation of Si-C-O-O with 2 nm of the SiO_x region in SiO_2/4H-SiC system as shown in Fig. 13 of the reference [35]. Replacing 1O by an N gives Si-C-O-N, adds a positive charge and double N_f at 23.5 x 10^{11}/cm^2, implying that N_f before NO annealing must be 12 x 10^{11}/cm^2. H_2 annealing after NO annealing adds H preferably to O than to C to give Si-C-O-N-H reducing N_f back to pre-annealed value as in wet re-oxidised oxide of 12 x 10^{11}/cm^2. Finally, replacing C-O-O by 3N due toN_2 annealing giving Si-N-N-N correlated bonds, and can also result in N_f of 23.5 x 10^{11}/cm^2. It can be observed that the number of electrons is the same in Si-C-O-N and Si-N-N-N and so will result in the same N_f value. A comparative study of defects in silicon nitride and SiO_2 suggests that the K^0 centre in Silicon Nitride is similar to the E' centre in SiO_2 with the energy level predicted to be near midgap of the nitride. Possibly, two K^0 defects produce a set of positive and negative centres [36]. The formation of SiCxOy at the SiC/SiO_2 interface is detected with the energy and number of electrons ejected from the top 10 nm surface having SiC2O2 bonds by high resolution XPS [37]. Another experimental study of 4H-SiC/SiO_2system summarises the formation of the correlated bonds [33]. All the correlated bonds discussed above are presented in Table III below.

Table III. N_f in p-type 4H-SiC MOS device for different atom combinations in the E' centre

Bond type	Si-C-O-O in SiO_2 on 4H-SiC after wet re-ox annealing at 950^{o}C for 3 hrs.	Si-C-O-O-H anneal in molecular H_2	Si-C-O-N anneal after wet re-ox with NO	Si-C-O-N-H anneal after NO with molecular H_2	Si-N-N-N anneal after wet re-ox with N_2 or N_2 plasma
Electrons	22 in C-O-O	23 in C-O-O-H	21 in C-O-N	22 in C-O-N-H	21 in N-N-N
N_f, (x 10^{11}/cm^2)	12	8	23.6	12	23.5

The above analysis results into the following inferences. One, the density of fixed charges from deep traps is obtained mostly in 4H-SiC MOS devices [38]. Two, the density of fixed charges due to excess Si or C that does not exchange charge with Si or SiC CB is low in 4H-SiC/SiO_2 system. Three, D_{it} is mainly P_b centres and deep donor or acceptor traps and D_{NIT} is density of border traps coming from the formation of E' centre and a positive charge centre after ionisation of neutral oxygen vacancy. Four, the border traps are dominant at low frequencies of <100 Hz and therefore quasi-static C-V alone can identify them well [5, 18, 19, 37, 39]. Five, the E' centre in the SiO_2 near the 4H-SiC/SiO_2 interface has 1C and 2O attached to the Si atom with an unpaired electron in place of 3O in the E' centre near the Si/SiO_2 interface because a minimum of 1C has to be there if SiC is used. Six, NO annealing to the saturation level replaces one O in C-O-O from the E' centre by N forming CN bonds. A high temperature N_2 annealing or N_2 plasma annealing can result in Si-N3 resulting in the same N_f in the p-type device of 23.5 x 10^{11}/cm^2. This N_f being related to the deep traps implies that D_{NIT} in this device is also the same as N_f. Seven, replacing O by C and then N in E' centre of thermal oxide (Si-O-O-O) results in adding positive charge and tripling or doubling N_f, respectively. Attaching H to O implies adding an electron or adding negative charges. Attaching an H to form Si-C-O-O-H results in addition of positive charges. Eight, the P_b centres are passivated with Si-N bonds reducing D_{it} by one order after NO annealing, but D_{NIT} doubles as compared to the wet re-ox condition. The D_{NIT} then goes back to the wet-re-ox value by H_2 annealing after NO annealing due addition of an electron from H forming a complex Si-C-O-N-H coordinated molecule. So, the surface effective mobility increases to35 cm^2/V-s after NO anneal because D_{it} is reduced by one order although D_{NIT} doubles [4]. Furthermore, H_2 annealing after NO annealing increases surface FE mobility to 55cm^2/V-s because D_{NIT} reduces back to pre-NO annealed value by adding H, and D_{it} is already reduced by N from NO annealing. This approach of NO annealing followed by H_2 annealing keeps the D_{NIT} to 12 x 10^{11}/cm^{2}eV. Annealing a dry oxide grown on n-type 4H-SiC epitaxial surface with low partial pressure of O_2 annealing (0.001% O_2) at 1300^{o}C to 1500^{o}C for 1 minute results in the E'centre as Si-C-O-O. A further H_2 annealing of this oxide can result in simpler correlated bonds as Si-C-O-O-H. The surface FE mobility however is not better than the NO + H_2 anneal condition because of higher D_{it} + D_{NIT} combined together. It needs to be kept in mind that D_{it} is distributed throughout the large bandgap of 4H-SiC of 3.23 eV making D_{it} reduction by one order by N as very significant [3]. Five different anneal conditions are compared based on the different device parameters and tabulated below in Table IV. The peak FE mobility of 55 cm^2/V-s obtained after NO + H_2 anneal is better and others are compared to it as worse. The device with N_2 anneal is a little worse but it is

competitive because of having strong Si-N3 bonds and the use of environment friendly N_2 gas [40]. It requires more energy to break N_2bonds having a bond strength of 9.8eV. Plasma N_2 and plasma $N_2 + H_2$ has been tried where electrical energy is partially substituted for thermal energy [41, 42]. It is not evaluated in this report. The concentration of carbon at the SiO_2/SiC interface is greater than $10^{20}/cm^3$, in the as-oxidised oxide after pure Ar anneal on n-4H-SiC MOS device and becomes $10^{18}/cm^3$ followed by O_2 anneal [20]. The volume density of carbon defects after oxygen anneal for a 2 nm interface is equal to surface density of 2 x $10^{11}/cm^2$.

Table IV. Comparison of five different annealing processes on SiO_2 based on the device parameters

Annealing condition	D_{it} at E_c-0.2 eV ($x10^{11}/cm^2eV$)	D_{NIT} ($x10^{11}/cm^2eV$)	$D_{it} + D_{NIT}$ D_{it} is throughout the bandgap ($x10^{11}/cm^2eV$)	Comparison of anneals	Surface FE mobility in n-channel MOSFET (cm^2/V-s)	Oxide breakdown field with charges (MV/cm)
As-oxidised	24	12	24 + 12	poor	5-7	>8
H_2 (400-1000°C)	24	6	24 + 6	O_2 + H_2 (worse)	27	>8
As-oxidised + NO at 1150°C or 1175°C for 2 hrs.	6	24	6 + 24	NO (good)	35-45 35 is effective mobility	≥7.8
H_2 after NO	6	12	6 + 12	NO + H_2 (better)	55	~5
As-oxidised + N_2 at 1300°C for 1-10 hrs.	2-10 (Avg. 6)	24	6 + 24	N_2 (Worse but competitive)	25-35	>8

Two possible solutions were thought to obtain lower D_{NIT} and N_f eventually did not prove effective. First, ozone oxidation was thought will remove C better because of an extra O in it. It does remove C but the final D_{it} atE_c-0.2 eV is still the same at 2 x $10^{12}/cm^2$eV.as after NO annealing [3, 43-44]. Second, the quality of the bulk 4H-SiC material and the epitaxial layer was questioned based on the premise that the oxide grown on a defective surface will yield poor quality oxide having larger oxygen vacancy concentration [6]. A study by Haney et al. [45] cleared the doubt about the poor quality of epitaxial layers. The n-channel MOSFETs fabricated on p-type epitaxial layers having thickness of 0.5 to 2µm resulted in the same surface mobility of $27cm^2/V$-s. In 4H-SiC MOS, after NO annealing and including N to the saturation level at the interface, N replaces O in the SiO_x. N having the atomic number of 7 has one less electron as compared to O having an atomic number of 8. So, replacing O by N adds positive charge to the SiO_x molecule. The NIT density after NO annealing in 4H-SiC MOS has become 23.5 x $10^{11}/cm^2$, which is one order higher than in Si/SiO_2 system as discussed earlier. It is possible to reduce D_{NIT} further by high temperature oxidation at 1300°C with 0.1% O_2 ambient as shown by N_f in n-type device [20], but at the expense of increasing D_{it} at E_c-0.2 eV. Also, the desirable NO annealing which reduces D_{it} will double the low D_{NIT} achieved as can be seen in Table IV above by comparing row 1 and 3. Higher D_{NIT} results in lower surface effective mobility in the MOSFETs such as 35 cm^2/V-s obtained by Chung et al. [4]. Furthermore, if one places more N forcefully than the planar density of Si (111) at the 4H-SiC/SiO_2 interface, some of the SiO_2 will become SiON having a lower bandgap [32]. The gate dielectric in the MOS device now becomes a stack of SiON/SiO_2. The author has already shown that a stack such as Al_2O_3/SiO_2 increases the leakage current and lowers the oxide breakdown field as compared to only having a thick oxide as gate dielectric [6]. However, in Si high-K metal gate (HKMG) technology and the other future technologies such as FinFET and Trigate, the high-K gate stack with ultrathin SiO_2 is needed to reduce the leakage current in the ultrathin SiO_2 layer. The amorphous high-K material such as HfO_2 with larger K value is able to effectively provide larger oxide thickness for the same capacitance and thus reduce the leakage current due to higher EOT of the stack. EOT is 1.4 nm in HKMG technology [6, 46].

In Si MOS device, superfine cleaning has shown interface trap density in mid $10^9/cm^2$ eV near mid gap of Si (can't find the reference but have read it). An oxide grown on such a surface could have lower number of oxygen vacancies created in the grown oxide which is the cause of formation of near interface traps or border traps and fixed charges by the formation of SiO_x. There densities could thus be possibly lowered, thereby increasing the surface effective and the field effect (FE) mobility in the MOSFETs. It has been suggested by Pantelides [47], that an abrupt Si/SiO_2 interface is possible. The author has tried a CF_4/H_2 plasma based silicon surface cleaning method with some success during his Ph.D. study at IT-BHU (IIT since 2012) during 1989-96 [48], where the flat band voltage resulted in a lower value due to replacement of native oxide by O_2 plasma oxide. This cleaning method was also investigated by Metzler et al. [49]. They found that the O content on the surface is reduced by more than 50% after the plasma oxidation as compared to more than 80% lower O content after HF etching. The surface reactivity after removing the native oxide immediately resulted in oxidation, whether the surface is at atmospheric pressure or at high vacuum condition [49]. H_2 rich plasma does not show re-oxidation after removal of the native oxide. It is still felt that the native oxide on Si surface formed during

the last rinsing process in de-ionised (DI) water after the HF etch can be replaced by another oxide and the author tried the use of O_2 plasma oxide, that could change the oxidation kinetics and improve the oxide quality in terms of lower oxygen vacancy concentration in the oxide and the oxide/Si interface. Of course, apart from the surface clean condition, the defect density at the semiconductor surface and in the bulk should also be kept low. It has been shown in 3C-SiC semiconductor having high defect density results in a poor quality grown oxide [6]. Si technology in this sense is very mature. The SiC or GaN technologies are still relatively less mature where epitaxial layers are used having lower defect densities.

The formula for the long-channel MOSFET ignoring channel length modulation due to short channel effects is given by:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}{}^2}{2}]$$

Here, I_{DS} is the drain to source current, μ_n is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, W is the width of the channel, L is the length of the channel, V_{GS} is the gate to source voltage, V_T is the threshold voltage of the MOSFET, and V_{DS} is the drain to source voltage. At low V_{DS} of say 50 mV, all the transfer curves of the MOSFET will have a common linear region. The field effect (FE) mobility can be obtained by partially differentiating the above formula for the current with V_{GS} while ignoring the last term in the above formula. It is given by:

$$\frac{\partial I_{DS}}{\partial V_{GS}} = g_m = \mu_n C_{ox} \frac{W}{L} V_{DS}$$

This gives the FE mobility as:

$$\mu_n = \frac{g_m}{C_{ox}} \frac{L}{W} \frac{1}{V_{DS}}$$

A 2008 report has shown that g_m in an n-channel 4H-SiC MOSFET increases with a reduced length of 1µm as compared to 3µm and increases the peak FE mobility to 50cm^2/V-s from 35cm^2/V-s after NO annealing [50]. However, it can be observed in the Fig 2(b) of the reference that this high mobility is available in a very narrow range of zero to 5 V of gate to source voltage and does not prove to be an effective way of increasing mobility. Although, the FE mobility for the NO + H_2 anneal is shown to be highest at 55 cm^2/V-s on the (0001) oriented surface, and the (1120) a-face oriented surface shows FE mobility of 100 cm^2/V-s of 4H-SiC-Si face, but the oxide breakdown reported is low at about 5MV/cm after H_2 anneal [51]. Another recent study on deposited oxide has improved mobility to 62cm^2/V-s after NO anneal by increasing the density of N at interface to 7.1 x 10^{20}/cm^3, as the midgap D_{it} reduced to 8.5 x 10^9/cm^2eV after NO annealing [52]. The N concentration at the interface is at 2 x 10^{14}/cm^2 after 2 hrs anneal time, in the present collaborative sample [53]. It can go up to the level of the PD of 8.1 x 10^{14}/cm^2 as shown in Table I above. It is shown to be a difficult feat with up to 6 hrs. of NO annealing at 1175^{o}C keeps the N concentration below 2 x 10^{14}/cm^2 [53]. A high temperature oxidation at 1300^{o}C to1500^{o}C has shown to reduce D_{NIT} as mentioned earlier but increases D_{it} near E_c-0.2 eV [20], and therefore must be increasing D_{it} thoughout the band gap. The increased D_{it} can however be passivated with N by NO anneal and at the same time double the reduced D_{NIT} by addition of positive charge due to replacement of O by N. This way, it is possible to increase FE mobility further. The bulk Hall mobility has been shown to be up to 300 cm^2/V-s for a 4H-SiC-Si face (0001) oriented surface with a doping of up to 10^{17}/cm^3 [54-55]. Potbhare et al. obtained a mobility of 250cm^2/V-s near the bottom of the inversion layer [56]. It is to be noted that the surface effective mobility comes from partially differentiating drain-source current with drain-source voltage while ignoring the last term, giving the channel conductance g_d at low V_{GS}-V_T voltage of say 5 to 10 volts. The surface carrier density of about10^{12}/cm^2 in inversion should be available to constitute the current. FE surface mobility is a bit lower than the surface effective mobility. The SiC power MOSFET has an application as a switch. It provides higher off-state voltage rating as compared to Si power MOSFET because of the wider bandgap of SiC that has lower intrinsic carrier density and can therefore withstand higher voltage. It is smaller in size and faster than the Si power MOSFET with and without SiC Schottky Barrier Diode (SBD) as it has much less reverse recovery charge. The use of this switch in DC to AC converter (Power Inverter) will improve the power conversion efficiency. Step-down cyclo-converter is a low frequency application for speed control of motor drives where D_{NIT} which is dominant at frequencies less than 100 Hz has relevance.

III. Conclusions

The surface mobility in an n-channel MOSFET on Si-face of 4H-SiC having (0001) orientation is limited by the high density of deep acceptor traps near the semiconductor CB represented by D_{NIT} in the text. Although D_{it} is significantly reduced, D_{NIT} is doubled after NO annealing because N replaces O and adds positive charge to the traps. D_{it} is distributed throughout the wide bandgap giving a large total interface trap density and N inclusion at the interface is desirable to reduce D_{it}. It is possible to reduce D_{NIT} by high temperature oxidation at the expense of increasing D_{it} at E_c-0.2 eV before NO annealing. It is possible to reduce D_{it} by increasing the N concentration at the interface. After NO annealing it is clear that the fixed charges are mainly due to deep traps and correlates with the neutral vacancies in the SiO_x region of 2-3 nm near the interface having Si-C-O-O correlated bonds after wet-re-oxidation. H_2 annealing after NO annealing has increased field effect surface mobility to 55cm^2/V-s but is causing degradation in oxide breakdown field with charges. A competitive device with N_2 anneal is possible with the use of environmentally friendly Nitrogen gas annealing, giving possibly E' centre as Si-N-N-N. Both, the D_{NIT} as well as D_{it} should be monitored while studying processing effects on mobility. Also, oxide breakdown should be monitored along with mobility because improving mobility could lead to lower oxide breakdown fields. The W/L ratio can increase the current in a MOSFET to give higher peak FE mobility, although it is applicable to small gate to source voltages only. Phonon-limited Hall bulk mobility of 300cm^2/V-s is the upper limit for surface mobility improvements on 4H-SiC semiconductor meant for power MOSFET switch application. The MOSFET has a higher off-state voltage rating, and is smaller and faster than the Si power MOSFET. It can improve the power conversion efficiency of power inverters or help control speed of motors. These are two applications of power MOSFETs.

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